Amendments to the Drawings:

The three attached sheets of drawings include formal drawings for Figures 3A-3E and minor changes to Figure 4. These sheets include Figures 3A-3E and 4, and replaces the original sheets including Figures 3A-3E and 4.

Attachment: three Replacement Sheets

REMARKS

Applicant respectfully requests reconsideration of this application, as amended, and consideration of the following remarks. Claims ___ have been amended. Claims ___ have been cancelled. Claims ___ remain pending. The drawings (Figures 3A-3E) are objected to because they are informal. The drawings are also objected to under 36 CFR 1.83(a) as not showing all of the claimed elements. Claims 1-11 stand rejected under 35 U.S.C.102(e) or in the alternative under 35 U.S.C. 103(a). Claims 12-20 stand rejected under 35 U.S.C. 103(a).

Amendments

Revisions to the Specification and Drawings

The Examiner requested formalization of the drawings containing Figures 3A-3E and Applicant hereby submits the formalized drawings. The Examiner also requests that all of the claimed elements were not illustrated. In response, Applicant has amended the specification in paragraph 65 and Figure 4. No new matter has been added as the amendments were supported in paragraphs 12-20 and claims 12-16 and 20 as originally filed. Accordingly, Applicant requests the objections to the drawings due to the noted informalities and under 36 CFR 1.83(a) and be withdrawn.

Amendments to the Claims

Applicant has amended the claims to more particularly point out what Applicant regards as the invention. [Summarize invention] No new matter has been added as a result of these amendments.

Rejections

Rejections under 35 U.S.C. §102(e) and 103(a)

Claims 1-11 stand rejected under 35 U.S.C.102(e) as anticipated or in the alternative, under 35 U.S.C. 103(a), as obvious in view of Price (US Pat 7,103,860) and as obvious in view of Killian (US Pat 6,760,888). Claims 12-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Price in view of Killian. Applicant respectfully traverses these rejections as set forth in more detail below.

Price discloses a program product for use in generating test benches for verifying test structures embedded in a circuit, comprises a verification specification processor for parsing a verification specification containing test specifications for selected test structures and a test bench generator for each of one or more types of embedded test structures, each test bench generator being operable to process a test structure specification of a test structure of a corresponding test structure type and generate a test bench using data contained in said test specifications of said verification specification, data contained in said test structure specification and data contained in a test connection specification.

The Examiner is relying on Price to teach or suggest a "product specification" and cites specifically to the follow excerpt:

> "Verification tool 100 further includes a test connection extraction module 110 which parses a circuit description 112 and generates a ***circuit test connection specification 114*** which identifies the test structures in the circuit. The ***test connection specification 114*** contains, for each test structure, the test structure name or identifier, the test structure type, the identity of a test structure specification and the identity of circuit ports to which test structure ports are connected." (Col 6, ln 58 – 65)

Accordingly, it appears that the Examiner is equating Price's "circuit test connection specification 114" to Applicant's "product specification". However, these two concepts are markedly different.

Referring now to Applicant's specification in paragraph 3 which defines and describes Applicant's "product specification":

> "Development devices are typically defined in a design document referred to as a product specification. By way of example, a product specification for an ASIC development device would define the required operations, I/O requirements and performance (e.g., speed, power and thermal efficiency). The ASIC device product specification can also include physical aspects of the development device (e.g., device size, circuit design, materials, manufacturing processes, etc.). As the development device is refined during the development cycle, the product specification is correspondingly refined."(Paragraph 3)

Applicant's "product specification" and Price's "circuit test connection specification 114" are clearly not the same nor even suggestive of one another as Price's "circuit test connection specification 114" is a data file specifically produced to drive a testing program. Applicant's "product specification" is a design and engineering document that goes well beyond the narrow focus of device testing.

Further, Price defines that the "circuit test connection specification 114 contains, for each test structure, the test structure name or identifier, the test structure type, the identity of a test structure specification and the identity of circuit ports to which test structure ports are connected." Applicant's design specification does not define a "test structure name or identifier, the test structure type, the identity of a test structure specification or the identity of circuit ports to which test structure ports are connected so therefore the Applicant's design specification and Price's circuit test connection specification 114 are not the same similar or even suggestive of one another.

The Examiner further seems to equate Price's "verification specification" with Applicant's product specification. According to the following excerpts of Price:

> "Verification tool 100 further includes a ***verification specification generator 120*** for generating a verification specification 103 and for storing the specification as an electronic file. The verification specification is preferably in the form of a text file which can be edited by a user using a text editor. Specification generator 120 groups test structures identified in a test connection specification 114 by test structure type with each test structure type group defining one or more test step specifications for one or more test structures of the same test structure type, and provides for each test structure group, global test structure type parameters and test step parameters for verifying test structures of said test structure type. This is described more fully later with reference to FIG. 7. ***FIG. 10 illustrates the content and structure of a verification specification according to a preferred embodiment of the invention***. The verification specification generator may also group test structures of each test structure type group into one or more sub-groups including hierarchical sub-groups, frequency sub-groups, and power consumption sub-groups." (Col 7, Ln 38-57, emphasis added)

Price's Figure 10 shows a verification specification as a specifically structured data file. Price's verification specification does not include nor suggest a product

specification. Applicant therefore submits that Applicant's product specification and Price's verification specification are not the same nor suggestive of one another.

Accordingly, Applicant submits that the rejections of claims 1-20 based on 35 U.S.C.102(e) or in the alternative, under 35 U.S.C. 103(a) as relates to Price should be withdrawn and claims 1-20 be found allowable over Price.

Killian diclsoses an automated processor design tool uses a description of customized processor instruction set extensions in a standardized language to develop a configurable definition of a target instruction set, a Hardware Description Language description of circuitry necessary to implement the instruction set, and development tools such as a compiler, assembler, debugger and simulator which can be used to develop applications for the processor and to verify it. Implementation of the processor circuitry can be optimized for various criteria such as area, power consumption, speed and the like. Once a processor configuration is developed, it can be tested and inputs to the system modified to iteratively optimize the processor implementation. By providing a constrained domain of extensions and optimizations, the process can be automated to a high degree, thereby facilitating fast and reliable development. In summary, Killian discloses a system of simulating a microprocessor design and testing the microprocessor design whether in hardware or in simulation.

Killian also does not teach or suggest a product specification as described by Applicant.

Accordingly, Applicant respectfully submits that Applicant's invention as claimed in claims 1-20 is neither anticipated by nor obvious in view of the cited references whether considered alone or in combination and respectfully request the withdrawal of the rejections under 35 U.S.C. § 102(e) and 103(a).

SUMMARY

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are in condition for allowance. Applicant respectfully requests reconsideration of the application and allowance of the pending claims.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact George B. Leavell at (408) 749-6900, ext 6923.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 50-0805 (Ref ADAPP263) for any charges that may be due or credit our account for any overpayment. Furthermore, if an extension is required, then Applicant hereby requests such extension.

Respectfully submitted,

MARTINE PENILLA & GENCARELLA, LLP

Dated: Jan. 22, 2006

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